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DSTATCOM Based Design and Analysis of Phase Shifted and Level Shifted Cascaded H-Bridge Multilevel Inverter for Power Quality Enhancement

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ABSTRACT
The Multilevel voltage source converters are issuing as a new engender of power converter choices for high power applications like in Distribution Static Compensator (DSTATCOM). In this paper presents a study of comparison between level shifted PWM and phase shifted PWM Cascaded H – bridge (CHB) Inverter as DSTATCOM in Power System (PS) for compensation of reactive power and harmonics. The DSTATCOM helps to improve the power factor and eliminate the Total Harmonics Distortion (THD) drawn from a Non-Linear Loads. The transient response of the DSTATCOM is very much important while compensating quickly changing unbalanced and nonlinear loads. Any change in the load affects the dc-link voltage directly. For this a fast acting dc link voltage controller used to generate the reference compensating currents for DSTATCOM. Finally a seven level of level shifted PWM and phase shifted PWM techniques are adopted to investigate the performance of CHB Inverter by using MATLAB/SIMULINK software.

Keywords – Cascaded Hybrid Bridge (CHB), DC-link voltage controller, DSTATCOM, fast transient response, harmonics, load compensation, power factor, power quality (PQ), unbalance, voltage-source inverter (VSI).

I. INTRODUCTION

Reactive power plays a vital role on the security and stability of power system, therefore, the reactive power compensation device has a very wide range of application in power system (PS). In recent years, technology of power electronics, PS especially distribution systems, have numerous non linear loads, which significantly affect the quality of power. Apart from non linear loads, events like capacitor switching, motor starting and unusual faults could also inflict power quality (PQ) problems. PQ problem is defined as any manifested problem in voltage/current or leading to frequency deviations that result in failure or mal-operation of customer equipment. Voltage sags and swells are among the many PQ problems the industrial processes have to face. Voltage sags are more severe. During the past few decades, power industries have proved that the adverse impacts on the PQ can be mitigated or avoided by conventional means, and that techniques using fast controlled force commutated power electronics (PE) are even more effective. PQ compensators can be categorized into two main types. One is shunt connected compensation device that effectively eliminates harmonics. The other is the series connected device, which has an edge over the shunt type for correcting the distorted system side voltages and voltage sags caused by power transmission system faults.

The STATCOM used in distribution systems is called DSTATCOM (Distribution-STATCOM) and its configuration is the same, but with small modifications. It can exchange both active and reactive power with the distribution system by varying the amplitude and phase angle of the converter voltage with respect to the line terminal voltage.

A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels. There are several types of multilevel inverters: cascaded H-bridge (CHB), neutral point clamped, flying capacitor [2-5]. In particular, among these topologies, CHB inverters are being widely used because of their modularity and simplicity. Various modulation methods can be applied to CHB inverters. CHB inverters can also increase the number of output voltage levels easily by increasing the number of H-bridges. In this paper presents transient response of the distribution static compensator (DSTATCOM) is very important while compensating rapidly varying unbalanced and nonlinear loads. Any change in the load affects the

dc-link voltage directly. The sudden removal of load would result in an increase in the dc-link voltage above the reference value, whereas a sudden increase in load would reduce the dc-link voltage below its reference value. The proper operation of DSTATCOM requires variation of the dc-link voltage within the prescribed limits. Conventionally, a proportional-integral (PI) controller is used to maintain the dc-link voltage to the reference value. It uses deviation of the capacitor voltage from its reference value as its input.

However, the transient response of the conventional PI dc-link voltage controller is slow. In this paper, a fast-acting dc-link voltage controller based on the energy of a dc-link capacitor is proposed. Finally a level shifted PWM (LSPWM) and phase shifted PWM (PSPWM) techniques are adopted to investigate the performance of CHB Inverter based DSTATCOM.

II. PRINCIPLE OF MULTILEVEL CHB INVERTER BASED DSTATCOM

A D-STATCOM (Distribution Static Compensator), which is schematically depicted in Figure- 1, consists of a two-level Voltage Source Converter (VSC), a dc energy storage device, a coupling transformer connected in shunt to the distribution network through a coupling transformer. The VSC converts the dc voltage across the storage device into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the D-STATCOM output voltages allows effective control of active and reactive power exchanges between the DSTATCOM and the ac system. Such configuration allows the device to absorb or generate controllable active and reactive power.

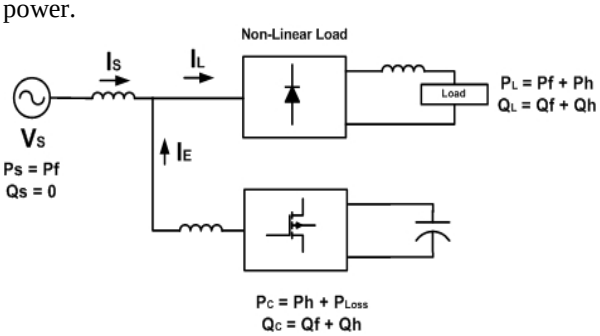

Figure 1: Basic two levels VSC based DSTATCOM.

The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes:

I. Voltage regulation and compensation of reactive power

2. Correction of power factor

3. Elimination of current harmonics.

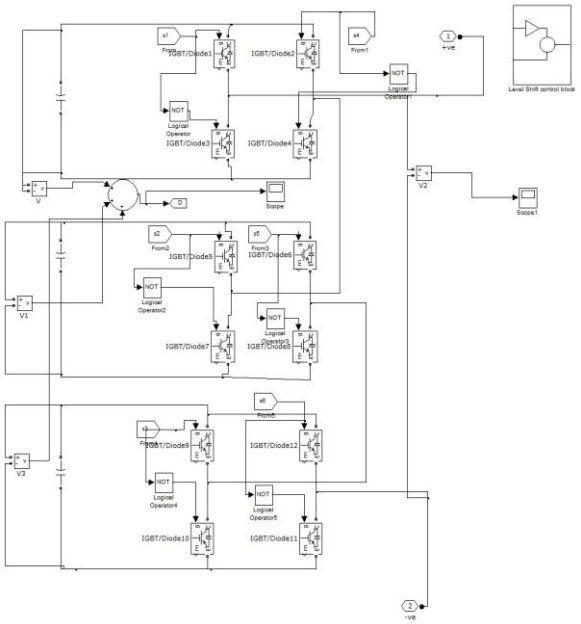

Figure 2: Seven level Cascaded H-Bridge Inverter per phase in DSTATCOM.

The operation of Distribution Static Compensator is simple and similar to the synchronous machine. It is well known that a synchronous machine can provide a lagging or leading current with respect to voltage by controlling the field current. In the same manner, we can vary the DC link voltage and control it. If the magnitude of voltage developed by DSTATCOM is larger than the three phase voltage, then the current shall flow from the DSTATCOM to the system. In this case, DSTATCOM acts as source of capacitive vars. In the second case, if the system voltage is larger than the voltage at the ac terminals of DSTATCOM, it behaves as an inductor. When if both the ac voltages at the system as well as the DSTATCOM are equal, then there is no reactive power exchange between the two.

III. DC LINK VOLTAGE CONTROLLERS

As mentioned before, the source supplies an unbalanced non- linear ac load directly and a dc load through the dc link of the DSTATCOM, as shown in Fig. 1. Due to transients on the load side, the dc bus voltage is significantly affected. To regulate this dc-link voltage, closed-loop controllers are used. The proportional-integral-derivative (PID) control provides a generic and efficient solution to many control problems. The control signal from PID controller to regulate dc link voltage is expressed as

$$u_c = K_p\,(V_{\mathrm{dc\,ref}} - v_{\mathrm{dc}}) + K_i \int (V_{\mathrm{dcref}} - v_{\mathrm{dc}})\mathrm{dt} + K_d\; d(V_{\mathrm{dc\,ref}} - v_{\mathrm{dc}})/\mathrm{dt}.$$

K_p, K_i *and* K_d is proportional, integral, and derivative gains of the PID controller, respectively. The proportional term provides overall control action proportional to the error signal. An increase in proportional controller gain reduces rise time and steady-state error but increases the overshoot and settling time. An increase in integral gain reduces steady- state error but increases overshoot and settling time. Increasing derivative gain will lead to improved stability. However, practitioners have often found that the derivative term can be against anticipatory action in case of transport delay. A cumbersome trial-and-error method to tune its parameters made many practitioners switch off or even exclude the derivative term [5-6]. Therefore, the description of conventional and the proposed fast-acting dc-link voltage controllers using PI controllers are given in the following subsections.

1. Conventional DC-Link Voltage Controller

The conventional PI controller used for maintaining the dc-link voltage is shown in Figure3. To maintain the dc-link voltage at the reference value, the dc-link capacitor needs a certain amount of real power, which is proportional to the difference between the actual and reference voltages. The power required by the capacitor can be expressed as follows:

$$P_{\mathrm{dc}} = K_p(V_{\mathrm{dc\,ref}} - v_{\mathrm{dc}}) + K_i \int (V_{\mathrm{dc\,ref}} - v_{\mathrm{dc}})\mathrm{dt}.$$

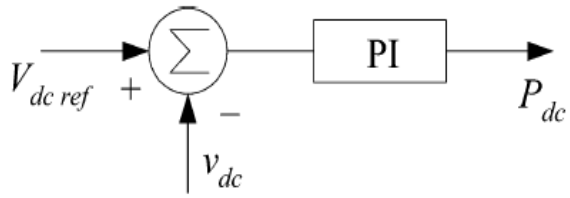

Figure 3: Schematic diagram of the conventional dc-link voltage controller.

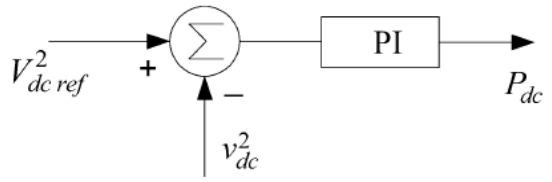

Figure 4: Schematic diagram of the fast-acting dc-link voltage controller.

The dc-link capacitor has slow dynamics compared to the compensator, since the capacitor voltage is sampled at every zero crossing of phase supply voltage. The sampling can also be performed at a quarter cycles depending upon the symmetry of the dc-link voltage waveform. The drawback of this conventional controller is that its transient response is slow, especially for fast-changing loads. Also, the design of PI controller parameters is quite difficult for a complex system and, hence, these parameters are chosen by trial and error. Moreover, the dynamic response during the transients is totally dependent on the values of K_p and K_i when P_{dc} is comparable to P_{lavg}.

2. Fast-Acting DC Link Voltage Controller

To overcome the disadvantages of the aforementioned controller, an energy-based dc-link voltage controller is proposed. The energy required by the dc-link capacitor (W_{dc}) to charge from actual voltage (V_{dc}) to the reference value ($V_{dc\ ref}$) can be computed as

$$W_{\mathrm{dc}} = \frac{1}{2} C_{\mathrm{dc}} \left(V^2_{\mathrm{dc\,ref}} - v^2_{\mathrm{dc}}\right)$$

In general, the dc-link capacitor voltage has ripples with double frequency, that of the supply frequency. The dc (*P' dc)* power required by the dc-link capacitor is given as

$$P'_{\mathrm{dc}} = \frac{W_{\mathrm{dc}}}{T_c} = \frac{1}{2T_c} C_{\mathrm{dc}} \left(V^2_{\mathrm{dc\,ref}} - v^2_{\mathrm{dc}}\right)$$

Where 'T_c' is the ripple period of the dc-link capacitor voltage, some control schemes have been reported in [10] and [12]. However, due to the lack of integral term, there is a steady-state error while compensating the combined ac and dc loads. This is eliminated by including an integral term. The input to this controller is the error between the squares of reference and the actual capacitor voltages. This controller is shown in Figure 4 and the total dc power required by the dc-link capacitor is computed as follows:

$$P_{\mathrm{dc}} = K_{\mathrm{pe}} \left(V^2_{\mathrm{dc\,ref}} - v^2_{\mathrm{dc}}\right) + K_{\mathrm{ie}} \int \left(V^2_{\mathrm{dc\,ref}} - v^2_{\mathrm{dc}}\right) \mathrm{dt}$$

The coefficients K_{pe} and K_{ie} are the proportional and integral gains of the proposed energy-based dc-link voltage controller.

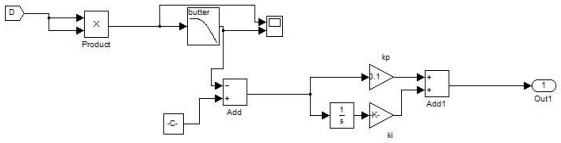

Figure 5: MATLAB/SIMULINK diagram of fast acting dc controller.

IV. PWM TECHNIQUES FOR CHB MULTILEVEL INVERTER

1. PHASE-SHIFT PWM method

CMC with m voltage levels requires (m – 1) triangular carriers. In the phase-shifted multi-carrier modulation, all the triangular carriers have the same frequency and the same peak- to-peak amplitude, but

there is a phase shift between any two adjacent carrier waves, given by:

$$\alpha = 360^0/ (m-1)$$

The gate signals are generated by comparing the modulating wave with the carrier wave. Figure 6 shows the principle of Phase shift PWM for one phase of seven levels CMC presented in Figure2 where six triangular wave carriers are required with a 60° phase displacement between any two adjacent carriers. The advantage of this method is that the switching frequency and conduction period is same for all devices and rotating of switching patterns is not required.

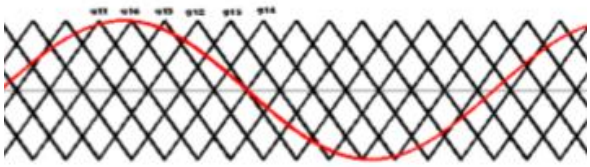

Figure 6: Phase shifted PWM for seven level CMC.

2. Level Shifted PWM Method

For m-level CMC using level-shifted multicarrier modulation scheme, (m – 1) triangular carriers are required, all having the same frequency and amplitude. The (m – 1) triangular carriers are vertically disposed such that the bands they occupy are contiguous. The amplitude modulation index is defined as:

$$m_a = \frac{V_m}{V_{cr}(m-1)}$$

Where Vm is the peak amplitude of the modulating wave and Vcr is the peak amplitude of each carrier wave. There are three schemes for level shift multi-carrier modulation listed as follows: 1. In-phase disposition (IPD), where all carriers are in phase. 2. Alternative phase opposite disposition (APOD), where all carriers are alternatively in opposite disposition. 3. Phase opposite disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference. In this paper only IPD modulation scheme is addressed as it provides the best harmonic profile of all three-level shift multi- carrier modulation schemes.

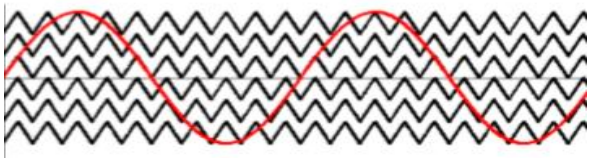

Figure 7: Level Shifted (IPD) seven level for CMC.

V. SIMULATION STUDIES

The load compensator with H-bridge VSI topology as shown in Figure 8 is realized by digital simulation by using MATLAB. The load and the compensator are connected at the distribution station. The ac load consists of a three-phase unbalanced load and three-phase diode bridge rectifier feeding a highly inductive R-L load. A dc load is realized by an equivalent resistance as shown in the figure8.

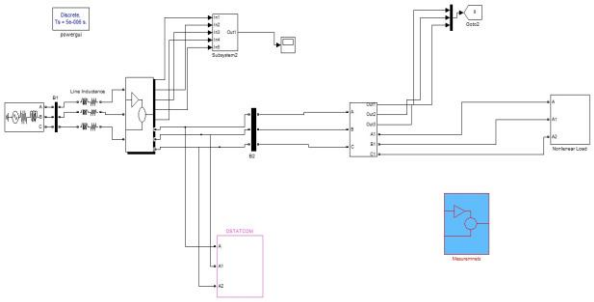

Figure 8: MATLAB/SIMULINK diagram of DSTATCOM at distribution station with non linear loads.

It consists of five blocks named as source block, non linear load block, control block, DSTATCOM block and measurements block. Here the simulation is carried out by three cases 1. Non-linear load without DSTATCOM and their THD in line currents, unbalance loads and 3rd & 5th harmonics, 2. Non-linear load with seven level Phase shift PWM cascaded multilevel DSTATCOM and their THD in line currents, unbalance loads and 3rd & 5th harmonics and 3. Non-linear load with seven level-Level shift PWM Cascaded multilevel DSTATCOM and their THD in line currents, unbalance loads and 3rd & 5th harmonics.

Table 1: system parameters

Source Voltage	11 KV & 50Hz
Line Resistance and inductance	0.01 ohm & 0.9e-3 H
DC bus capacitance	1550e-6 F
Inverter Series inductance	10e-3 H
Load resistance and Inductance	60 ohm (one more 60ohm's add for unbalance load condition) & 10e-3 H
Non-linear load	3 arms Diode bridge

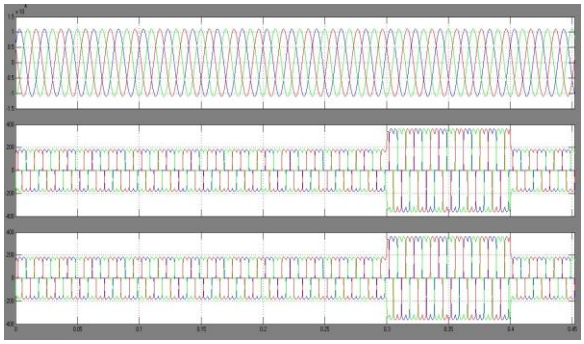

Figure 9: Without DSTATCOM results of source voltage, source current and load current.

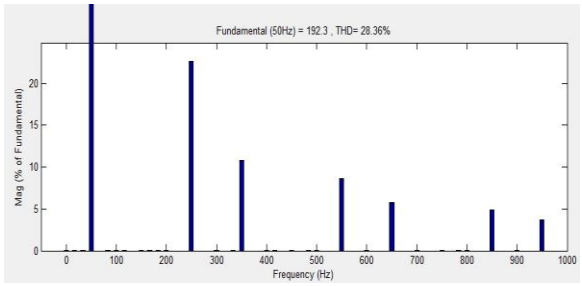

Figure 10: THD value in line current without DSTATCOM.

Figure 9 & 10 shows the without DSTATCOM results and THD Value in %, clearly shown unbalanced load (0.3 sec to 0.4 sec) in figure 9. THD value is 28.36%, 3rd harmonic is 0.00% and 5th harmonic is 22.60%.

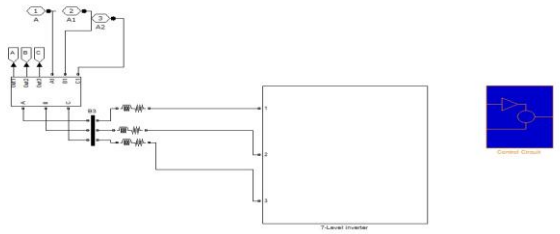

Figure 11: DSTATCOM sub block with control block & 7-level CHB inverter.

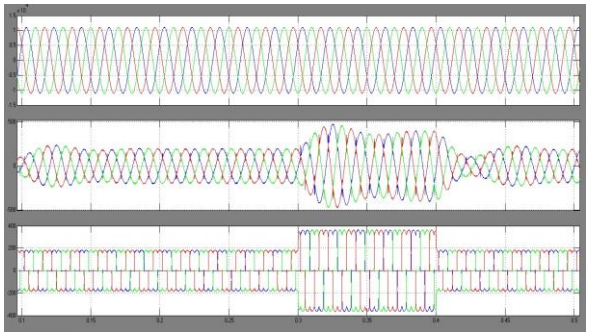

Figure 12: With DSTATCOM seven level- Level shift PWM technique of CHB inverter results 1) Source Voltage 2) Source current & 3) Load current.

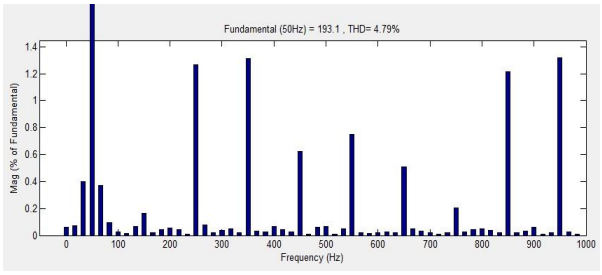

Figure 13: THD value in line current of seven level-level shift PWM CHB inverter.

Figure 12 & 13 shows the with DSTATCOM seven level- Level shift PWM CHB inverter results and THD Value in %, THD value is 4.79%, 3rd harmonic is 0.16% and 5th harmonic is 1.27%.

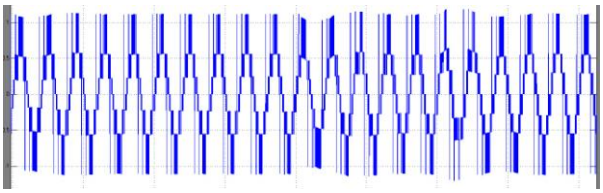

Figure 14: Seven level-Level shift inverter result.

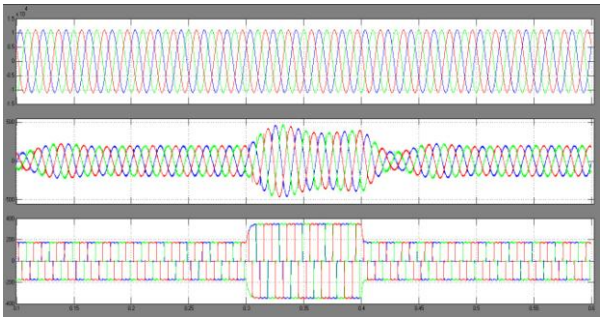

Figure 15: With DSTATCOM seven level-Phase shift PWM technique of CHB inverter results 1) Source Voltage 2) Source current & 3) Load current.

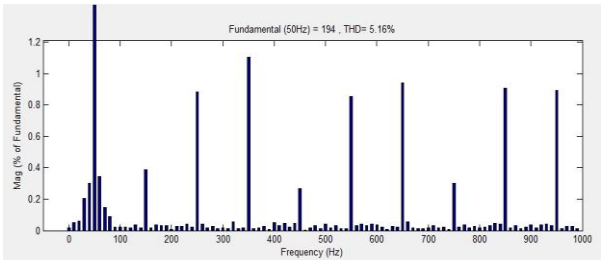

Figure 16: THD value in line current of seven level-level shift PWM CHB inverter.

Figure 15 & 16 shows the with DSTATCOM seven level- Phase shift PWM CHB inverter results and THD Value in %, THD value is 5.16%, 3rd harmonic is 0.39% and 5th harmonic is 0.88%.

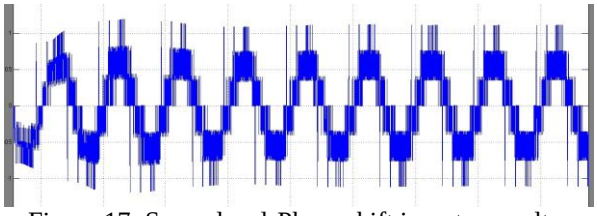

Figure 17: Seven level-Phase shift inverter result.

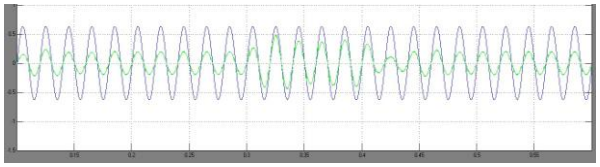

Figure 18: Phase A Voltage in phase with current.

Table 2: Comparison between the Level Shift PWM and Phase shift PWM Techniques.

Comparison	Level shift PWM	Phase shift PWM
Device switching frequency	Different	Same for all devices
Device conduction period	Different	Same for all devices
THD	4.79 %	5.16%
3rd harmonic content	0.16%	0.39%
5th harmonic content	1.27%	0.88%

VI. CONCLUSION

DSTATCOM with proposed fast acting dc link voltage controller improves transient response, reduces harmonics and provides reactive power compensation due to unbalance loads, non linear loads and voltage variations in distribution system. A seven level CHB multilevel inverter based DSTATCOM with Level shift PWM and phase shift PWM techniques are invested on nonlinear loads and unbalanced loads conditions by MATLAB/ SIMULINK results and total harmonics distortion under unbalance loads and non linear loads condition. As evident from the simulation studies, dc bus capacitor voltage settles early and an energy-based fast-acting dc-link voltage controller is suggested to ensure the fast transient response of the compensator. The THD of the source current is investigated for both Phase shift PWM and level shift PWM for a seven level inverter based DSTATCOM. THD simulation results under non-linear loads are investigated and found that the Level shift PWM results are better than Phase shift PWM.

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Biography

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